RADIOMETRIX

Hartcran House, 231 Kenton Lane, Harrow, Middlesex, HA3 8RP, England
Tel: +44 (0) 20 8909 9595, Fax: +44 (0) 20 8909 2233, www.radiometrix.com

RMX2

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NBFM Direct Interface Multi Channel Transceiver

The RMX2 is an ETSI EN 300 220-3 compliant UHF FM narrow band semi-duplex radio data module. It is a high performance transceiver designed for use in industrial applications requiring long range, high performance and reliability.
The operating frequencies are available in the 315MHz, 433.05-434.79MHz European ISM band and 458.5-459.1MHz UK SRD band allocations.

Figure 1: RMX2-433-10

Features

- +10dBm (10mW) RF power, 3.0V @ 35mA operation
- Programmable RF channel
- Fast TX/RX switching time (5ms)
- Receiver sensitivity -119dBm
- Class one receiver performance
- ETSI EN 300 220-3, EN 301 489-3 compliant

RMX2 is a narrowband multichannel module with 25 kHz channel steps, but still achieves sub-10mS TX/RX switching speed, making it an ideal RF unit for inclusion in feedback systems.

The narrow band technique used in RMX2 enables high interference rejection and concurrent operation with multiple modules.

Applications

Telemetry

- Water level monitor for rivers, dams, etc.
- Monitoring systems for environmental data such as temperature, humidity, etc.
- Transmission of measurement data (pressure, revolution, current, etc) to PC
- Security alarm monitoring

Telecontrol

- Industrial remote control systems
- Remote control systems for factory automation machines

***Evaluation platforms**: NBEK + RMX carrier*

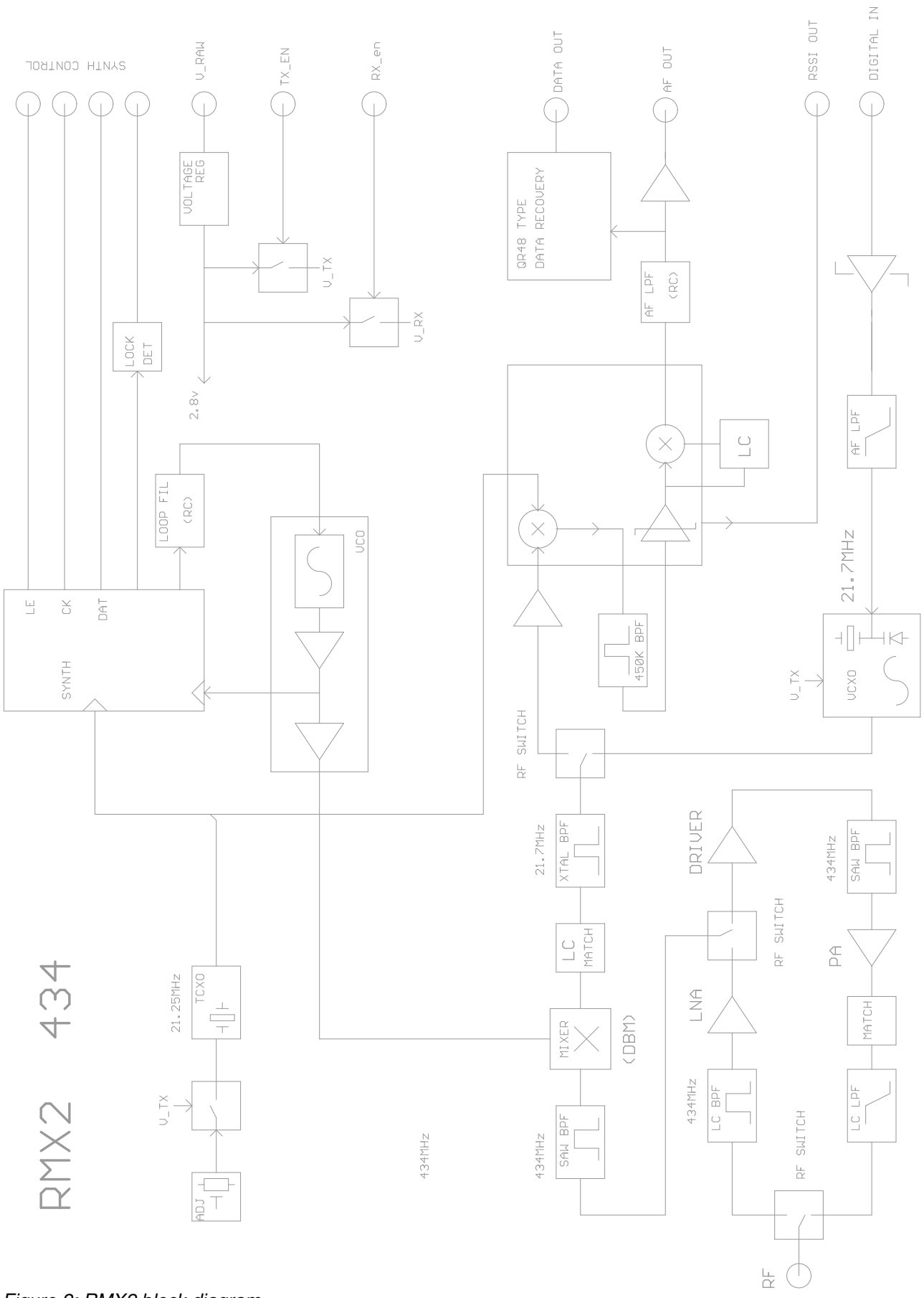
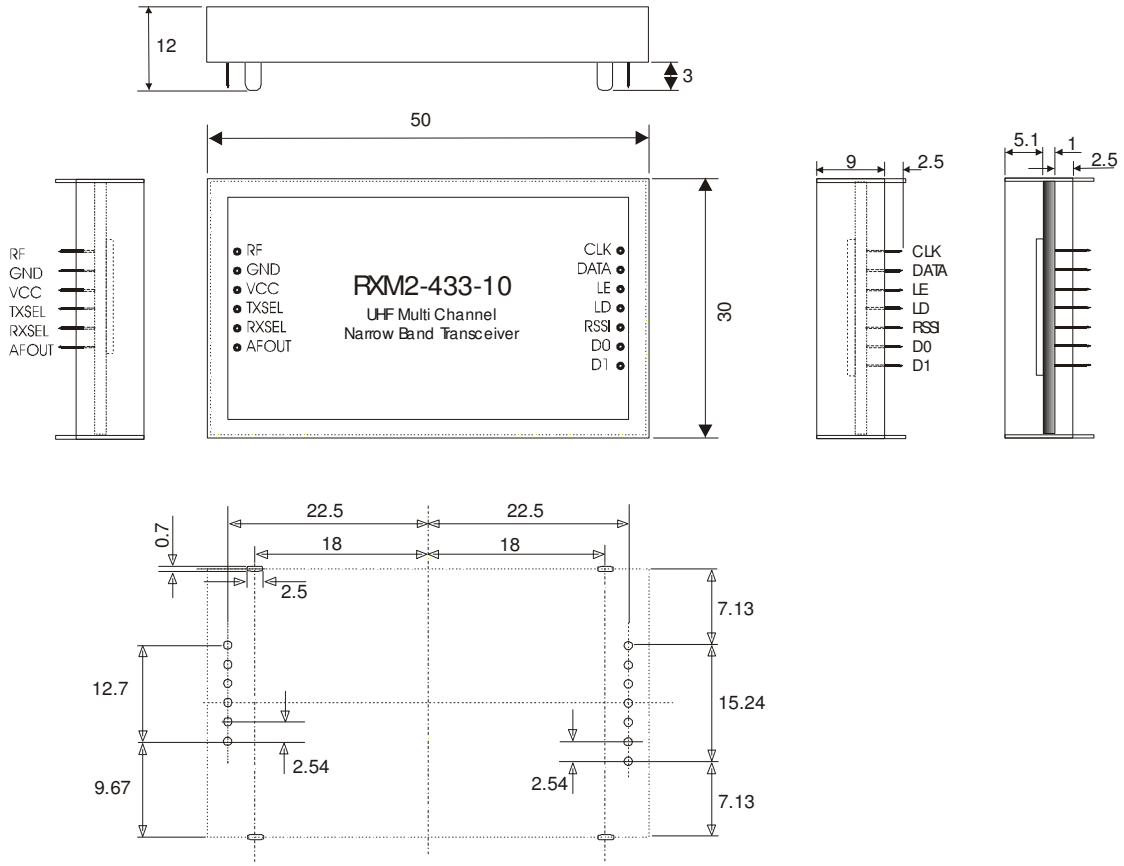


Figure 2: RMX2 block diagram



Reference hole position for PCB mounting (bottom view)

recommended PCB hole size: 1.2 mm
pin pitch: 2.54 mm
module footprint size: 30 x 50 mm

Figure 3: Pinouts and dimensions

Condensed specifications

All ratings at 25℃ unless otherwise noted

Parameter	Rating	Conditions
General characteristics		
Operating frequency range	315 - 315.375 MHz	
	433.05 - 434.775 MHz	European ISM band (RMX2-433-10)
	458.5 - 459.1MHz	UK SRD allocation (RMX2-458-10)
Channel step	Programmable (PLL IC: Fujitsu MB15E03SL)	
Frequency stability	±3ppm	-20 to +70 ℃
Data rate	9600 bps max	Input data pulse width: Min 104µs, Max 5ms
PLL reference frequency	21.25 MHz	
Operating voltage range	3 – 15 V	
Supply Current	35mA (TX) 24mA (RX)	
Operating temperature range	- 20 to + 70 ℃	
Dimensions	30 x 50 x 9 mm	
Transmitter section		
RF output power	10mW ±1dB	At 434.0MHz / 458.7MHz, Antenna impedance 50Ω
Deviation (Digital In)	2.4kHz ±0.3kHz	PN9, 9600 bps, LPF 20 kHz
Deviation frequency characteristics	± 3dB	DC to 4800Hz
TX S/N	-30dB	1kHz, Deviation = ±2.4kHz CCITT filter
Spurious emission	<-54dBm	<1GHz, non-harmonic spurii
	<-40dBm	2nd and 3rd harmonics
Adjacent channel leakage power	-37dBm	CH 25kHz, BW = 16kHz, PN9, 9600 bps
Total distortion and noise	30dB	1kHz, Deviation = ±2.4kHz, CCITT filter
Switching time RX to TX	5 - 10ms	RX → TX [*1]
Lock time	30 – 40ms	Free Run → TX [*2]
	10 – 20ms	25kHz channel shift [*3]
Receiver section		
Receiver Sensitivity	-119dBm (AF OUT)	1kHz, Deviation ±2.4kHz, CCITT filter
Receiver S/N	35dB	1kHz, Deviation ±2.4 kHz, CCITT filter, RF level = -30dBm
Distortion	5%	1kHz, Deviation ±2.4kHz, CCITT filter, RF level=-30dBm
All spurious responses	Better than 60dB	2 signal method, Jamming signal = FM
Intermodulation	Better than 50dB	2 signal method
Adjacent channel selectivity	65dB	2 signal method, ± 25kHz Jamming signal = FM
Blocking	>84dBm	± 1, 2, 5, 10 MHz
Switching time TX to RX	5 - 10 ms	TX → RX [*1]
Lock Time	30 - 40 ms	Free Run → RX [*2]
	10 - 20 ms	25kHz channel shift [*3]

NOTES:

1. Time until TX frequency or 1st Local frequency reach a steady frequency ±1.5ppm
2. Time until TX frequency or 1st Local frequency reach a steady frequency ±1.5ppm after PLL setting data is set.
3. Time until TX frequency or 1st Local frequency reach a steady frequency ±1.5ppm after setting PLL setting data to change the frequency for 25kHz

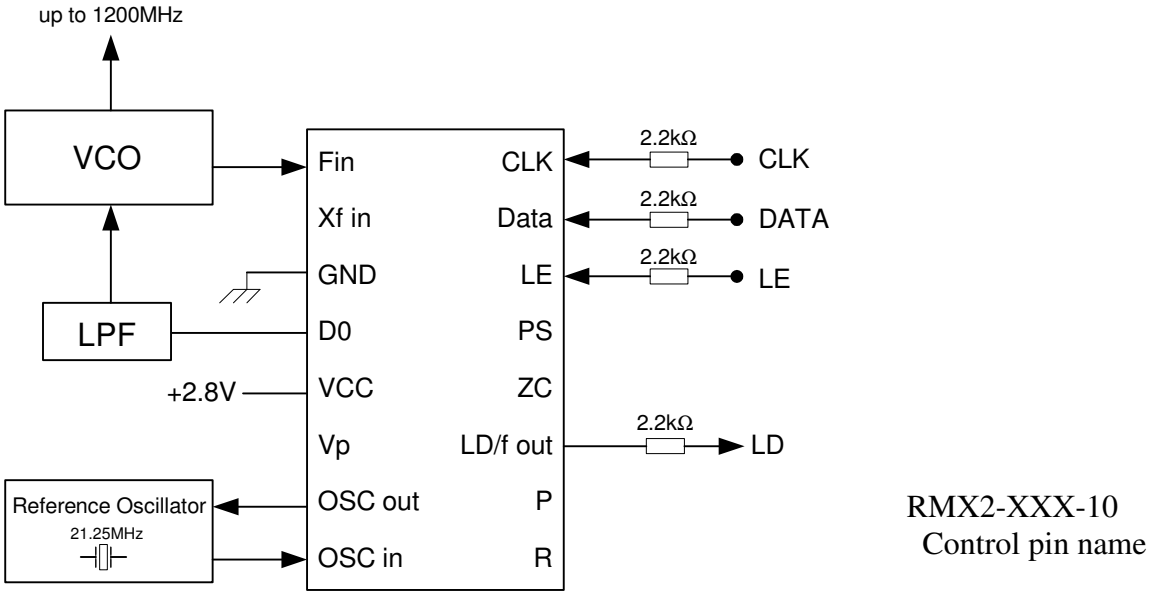


Figure 4: PLL IC Control

RMX2 has an internal PLL frequency synthesizer as shown in Figure 1. Channel frequency is set by loading data directly into the registers of the controlling IC over a simple, 3 wire serial bus (interface pins CLK, LE, DATA). Also RMX2 has a Lock Detect (LD) terminal that shows the lock status of the frequency. These signal lines are connected directly to the PLL IC through a 2.2kΩ resistor.

The interface voltage of RMX2 is 2.8 V, so the control voltage must be the same. RMX2 comes equipped with a Fujitsu MB15E03SL PLL IC. Please refer to the manual of the PLL IC.
http://www.fujitsu.com/downloads/MICRO/fme/pll/e421359.pdf

The following is a supplementary description related to operation with RMX2. In this description, the same names and terminology as in the PLL IC manual are used, so please read the manual beforehand.

How to calculate the setting values for the PLL register

The PLL IC manual shows that the PLL frequency setting value is obtained with the following equation.

$$f_{VCO} = \frac{[(M \times N) + A] \times f_{OSC}}{R} \qquad N > M^2 \qquad \textbf{Equation 1}$$

f_{vco} : Output frequency of external Voltage Controlled Oscillator (VCO)
N: Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \le A \le 127$)
f_{osc}: Output frequency of the reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)
M: Preset divide ratio of the dual modulus prescaler (64 or 128)

Because of the circuitry used in the RMX2, the frequency programmed into the PLL must be 21.7MHz below the desired channel frequency. There is no need to re-program when switching between transmit and receive modes.
Therefore the expected value of the frequency generated at VCO (fexpect) is as below.

fvco = fexpect = (fch – 21.7MHz) ***Equation 2***

The PLL generates channel frequencies as multiples of a 'comparison' frequency. This phase comparison frequency (fcomp) is made by dividing the frequency input to the PLL from the reference oscillator by reference counter R. The RMX2 uses a 21.25 MHz TCXO for the reference clock fosc.
fcomp can be either 12.5kHz or 25 kHz.

The above equation 1 results in the following with n = M x N + A, where “n” is the number for division.

$$f_{VCO} = n \times f_{comp} \qquad \textbf{Equation 3}$$

$$n = \frac{f_{VCO}}{f_{comp}} \qquad \text{note: } f_{comp} = \frac{f_{OSC}}{R} \qquad \textbf{Equation 4}$$

Also, this PLL IC operates with the following R, N, A and M relational expressions.

$$R = \frac{f_{OSC}}{f_{comp}} \qquad \textbf{Equation 5}$$

$$N = INT\left(\frac{n}{M}\right) \qquad \text{INT: Integer portion of a division} \qquad \textbf{Equation 6}$$

$$A = n - (M \times N) \qquad \textbf{Equation 7}$$

As an example, the setting value of RF channel frequency f_{ch} 434.6750MHz can be calculated as below.

Conditions:	Channel center frequency:	f_{ch} = 434.6750MHz
Constant:	Offset frequency:	f_{offset}=21.7 MHz
Constant:	Reference frequency:	f_{osc}=21.25 MHz

Set 25 kHz for Phase Comparison Frequency f_{comp} and 64 for Prescaler value M

The frequency of VCO will be:
$f_{vco} = f_{expect} = f_{ch} - f_{offset}$ = 434.675 –21.7 = 412.975MHz

Dividing value “n” is derived from Equation 4
$n = f_{vco} / f_{comp}$ = 412.975MHz/25kHz = 16519
Value “R” of the Reference Counter is derived from Equation 5.
$R = f_{osc}/f_{comp}$ = 21.25MHz/25kHz = 850
Value “N” of the programmable counter is derived from Equation 6.
N = INT (n/M) = INT(16519/64) = 258
Value “A“ of the swallow counter is derived from Equation 7.
A = n – (M x N) = 16519 – 64 x 258 = 7

The frequency of RMX2 is locked at a centre frequency f_{ch} by inputting the PLL setting values N, A and R obtained with the above equations as serial data. The above calculations are the same for the other frequencies.

Method of serial data input to the PLL

After the RF channel table plan is decided, the data needs to be allocated to the ROM table and read from there or calculated with the software.

Together with this setting data, operation bits that decide operation of the PLL must be sent to the PLL. The operation bits for setting the PLL are as follows. These values are placed at the head of the reference counter value and are sent to the PLL.

CS: Charge pump current select bit
CS = 0 ±1.5 mA select VCO is optimised to ±1.5 mA

LDS: LD/fout output setting bit
LDS = 0 LD select Hardware is set to LD output

FC: Phase control bit for the phase comparator
FC = 1 Hardware operates at this phase

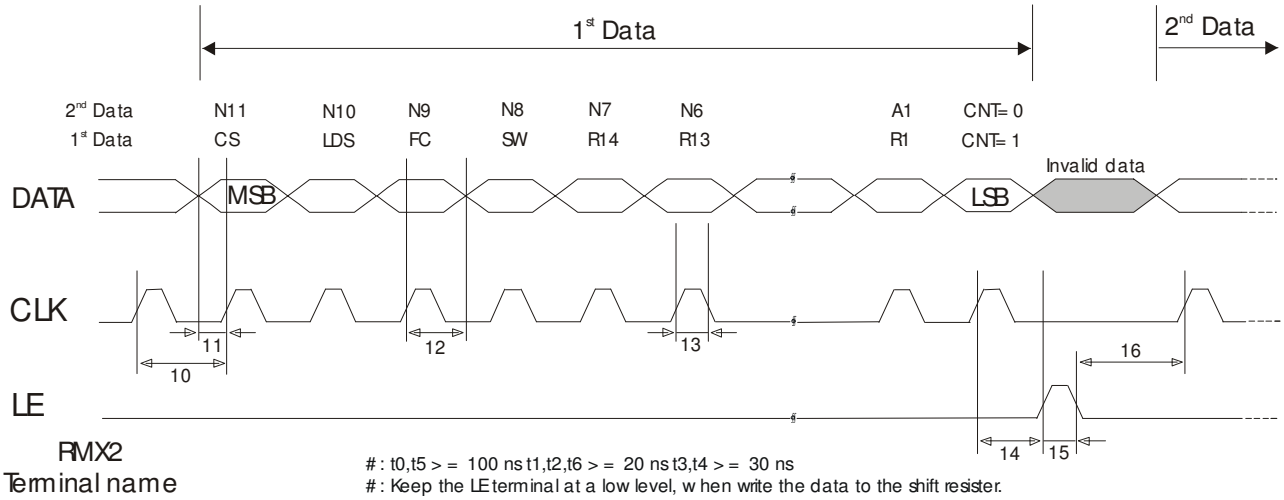


Figure 5: PLL IC programming timing diagram

The PLL IC, which operates as shown in the block diagram in the manual, shifts the data to the 19-bit shift register and then transfers it to the respective latch (counter, register) by judging the CNT control bit value input at the end.

CLK [Clock]:	Data is shifted into the shift register on the rising edge of this clock.
LE [Load Enable]:	Data in the 19-bit shift register is transferred to respective latches on the rising edge of the clock. The data is transferred to a latch according to the control bit CNT value.
Data [Serial Data]:	You can perform either reference counter setup or programmable counter setup first.

TIMING CHART

Control timing in a typical application is shown in Figure 3.

Initialisation of the radio is performed following power-up and successful reset of the controlling CPU. The FET switches controlling the radio module systems (controlled by RXSEL and TXSEL) must be set to inactive (pin high or floating) to avoid unwanted emissions.

The power supply to the radio module is then turned on. When the radio module is first powered, the PLL internal registers are not yet set to meaningful values, and the VCO circuit will be unstable.
Data transmission and reception is only possible 40 ms after the first set up data is sent to the PLL.
Subsequent 'channel change' re-programming only takes 20 ms before data can be handled.

Changing channels must be carried out in the receive mode. If switching is performed in transmission mode, unwanted interference will be generated.

If the module is switched to the receive mode when operating in the same channel, (a new PLL setting is not necessary) it can receive data within 5 ms of switching*1. For data transmission, if the RF channel to be used for transmission is set while still in receiving mode, data can be sent at 5 ms after the radio module is switched from reception to transmission*2.

Check that the Lock Detect signal is "high" 20 ms after the channel is changed. In some cases the Lock Detect signal becomes unstable before the lock is correctly detected, so it is necessary to note if processing of the signal is interrupted.

*1: DC offset may occur due to frequency drift caused by ambient temperature change. Customers are urged to verify operation at low temperature and □nitiali their timing.

*2: Sending '10101…..' preamble just after switching to transmission mode enables smoother operation of the data extraction circuit used by the receiver.
For 9600 bps, a preamble of '11001100' is effective.
Recommended preamble length:
-10 ℃ -+55℃: 7 ms
-20 ℃ - +65 ℃ (for operation exceeding the above range): 15 ms

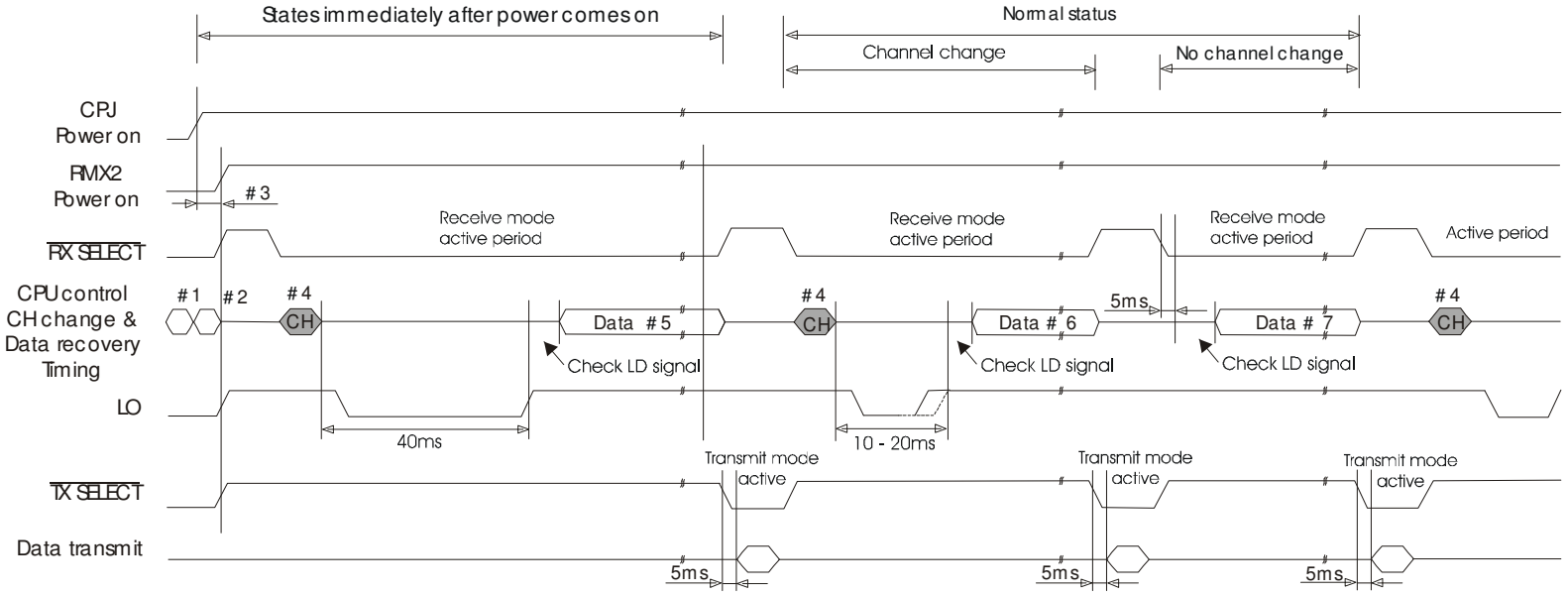


Figure 6: Timing diagram for RMX2

#:1 Reset control CPU

#:2 Initialize the port connected to the module.

#:3 Supply pow er to the module after □nitialising CPU.

#:4 Rfchannel change must be performed in receiving mode.

#:5 40 ms later, the receiver can receive the data after changing the channel..

#:6 10 to 20 ms later, the receiver can receive the data after changing the channel.

#:7 5 ms later, the data can be received if the RF channel is not changed.

PLL frequency setting data reference

RMX2-433-10: 433MHz European ISM band (433.050 – 434.790 MHz)

Parameter name	Value
Phase Comparing Frequency F_{comp} [kHz]	25
Start Channel Frequency F_{ch} [MHz]	433.0750
Channel Step Frequency [kHz]	25
Number of Channel	69
Prescaler M	64

Parameter name	Value
Reference Frequency F_{OSC}[MHz]	21.25
Offset Frequency F_{offset} [MHz]	21.7

: For data input
: Result of calculation
: Fixed Vale

Parameter name	Value
Reference Counter R	850
Programmable Counter N Min. Value	257
Programmable Counter N Max. Value	258
Swallow Counter A Min. Value	0
Swallow Counter A Max. Value	63

CH. No.	Channel Frequency F_{ch} (MHz)	Expect Frequency F_{expect} (MHz)	Lock Frequency F_{VCO} (MHz)	Number of Division n	Programmable Counter N	Swallow Counter A
0	433.0750	411.3750	411.3750	16455	257	7
1	433.1000	411.4000	411.4000	16456	257	8
2	433.1250	411.4250	411.4250	16457	257	9
3	433.1500	411.4500	411.4500	16458	257	10
4	433.1750	411.4750	411.4750	16459	257	11
5	433.2000	411.5000	411.5000	16460	257	12
6	433.2250	411.5250	411.5250	16461	257	13
7	433.2500	411.5500	411.5500	16462	257	14
8	433.2750	411.5750	411.5750	16463	257	15
9	433.3000	411.6000	411.6000	16464	257	16
10	433.3250	411.6250	411.6250	16465	257	17
11	433.3500	411.6500	411.6500	16466	257	18
12	433.3750	411.6750	411.6750	16467	257	19
13	433.4000	411.7000	411.7000	16468	257	20
14	433.4250	411.7250	411.7250	16469	257	21
15	433.4500	411.7500	411.7500	16470	257	22
16	433.4750	411.7750	411.7750	16471	257	23
17	433.5000	411.8000	411.8000	16472	257	24
18	433.5250	411.8250	411.8250	16473	257	25
19	433.5500	411.8500	411.8500	16474	257	26
20	433.5750	411.8750	411.8750	16475	257	27
21	433.6000	411.9000	411.9000	16476	257	28
22	433.6250	411.9250	411.9250	16477	257	29
23	433.6500	411.9500	411.9500	16478	257	30
24	433.6750	411.9750	411.9750	16479	257	31
25	433.7000	412.0000	412.0000	16480	257	32
26	433.7250	412.0250	412.0250	16481	257	33
27	433.7500	412.0500	412.0500	16482	257	34
28	433.7750	412.0750	412.0750	16483	257	35
29	433.8000	412.1000	412.1000	16484	257	36
30	433.8250	412.1250	412.1250	16485	257	37
31	433.8500	412.1500	412.1500	16486	257	38
32	433.8750	412.1750	412.1750	16487	257	39

33	433.9000	412.2000	412.2000	16488	257	40
34	433.9250	412.2250	412.2250	16489	257	41
35	433.9500	412.2500	412.2500	16490	257	42
6	433.9750	412.2750	412.2750	16491	257	43
37	434.0000	412.3000	412.3000	16492	257	44
38	434.0250	412.3250	412.3250	16493	257	45
39	434.0500	412.3500	412.3500	16494	257	46
40	434.0750	412.3750	412.3750	16495	257	47
41	434.1000	412.4000	412.4000	16496	257	48
42	434.1250	412.4250	412.4250	16497	257	49
43	434.1500	412.4500	412.4500	16498	257	50
44	434.1750	412.4750	412.4750	16499	257	51
45	434.2000	412.5000	412.5000	16500	257	52
46	434.2250	412.5250	412.5250	16501	257	53
47	434.2500	412.5500	412.5500	16502	257	54
48	434.2750	412.5750	412.5750	16503	257	55
49	434.3000	412.6000	412.6000	16504	257	56
50	434.3250	412.6250	412.6250	16505	257	57
51	434.3500	412.6500	412.6500	16506	257	58
52	434.3750	412.6750	412.6750	16507	257	59
53	434.4000	412.7000	412.7000	16508	257	60
54	434.4250	412.7250	412.7250	16509	257	61
55	434.4500	412.7500	412.7500	16510	257	62
56	434.4750	412.7750	412.7750	16511	257	63
57	434.5000	412.8000	412.8000	16512	258	0
58	434.5250	412.8250	412.8250	16513	258	1
59	434.5500	412.8500	412.8500	16514	258	2
60	434.5750	412.8750	412.8750	16515	258	3
61	434.6000	412.9000	412.9000	16516	258	4
62	434.6250	412.9250	412.9250	16517	258	5
63	434.6500	412.9500	412.9500	16518	258	6
64	434.6750	412.9750	412.9750	16519	258	7
65	434.7000	413.0000	413.0000	16520	258	8
66	434.7250	413.0250	413.0250	16521	258	9
67	434.7500	413.0500	413.0500	16522	258	10
68	434.7750	413.0750	413.0750	16523	258	11

RMX2-458-10: 458MHz UK SRD band (458.525 – 459.175 MHz)

Parameter name	Value
Phase Comparing Frequency F_{comp} [kHz]	25
Start Channel Frequency F_{ch} [MHz]	458.5250
Channel Step Frequency [kHz]	25
Number of Channel	27
Prescaler M	64

Parameter name	Value
Reference Frequency F_{OSC}[MHz]	21.25
Offset Frequency F_{offset} [MHz]	21.7

: For data input
: Result of calculation
: Fixed Vale

Parameter name	Value
Reference Counter R	850
Programmable Counter N Min. Value	273
Programmable Counter N Max. Value	273
Swallow Counter A Min. Value	1
Swallow Counter A Max. Value	27

CH No.	Channel Frequency F_{ch} (MHz)	Expect Frequency F_{expect} (MHz)	Lock Frequency F_{VCO} (MHz)	Number of Division n	Programmable Counter N	Swallow Counter A
0	458.5250	436.8250	436.8250	17473	273	1
1	458.5500	436.8500	436.8500	17474	273	2
2	458.5750	436.8750	436.8750	17475	273	3
3	458.6000	436.9000	436.9000	17476	273	4
4	458.6250	436.9250	436.9250	17477	273	5
5	458.6500	436.9500	436.9500	17478	273	6
6	458.6750	436.9750	436.9750	17479	273	7
7	458.7000	437.0000	437.0000	17480	273	8
8	458.7250	437.0250	437.0250	17481	273	9
9	458.7500	437.0500	437.0500	17482	273	10
10	458.7750	437.0750	437.0750	17483	273	11
11	458.8000	437.1000	437.1000	17484	273	12
12	458.8250	437.1250	437.1250	17485	273	13
13	458.8500	437.1500	437.1500	17486	273	14
14	458.8750	437.1750	437.1750	17487	273	15
15	458.9000	437.2000	437.2000	17488	273	16
16	458.9250	437.2250	437.2250	17489	273	17
17	458.9500	437.2500	437.2500	17490	273	18
18	458.9750	437.2750	437.2750	17491	273	19
19	459.0000	437.3000	437.3000	17492	273	20
20	459.0250	437.3250	437.3250	17493	273	21
21	459.0500	437.3500	437.3500	17494	273	22
22	459.0750	437.3750	437.3750	17495	273	23
23	459.1000	437.4000	437.4000	17496	273	24
24	459.1250	437.4250	437.4250	17497	273	25
25	459.1500	437.4500	437.4500	17498	273	26
26	459.1750	437.4750	437.4750	17499	273	27

Note: In the 458MHz SRD band in the UK, channel frequencies 458.825MHz, 458.8375MHz and 458.900MHz are reserved for alarm usage, and should not be used for general telemetry applications

Radiometrix Ltd
Hartcran House
231 Kenton Lane
Harrow, Middlesex
HA3 8RP
ENGLAND
Tel: +44 (0) 20 8909 9595
Fax: +44 (0) 20 8909 2233
sales@radiometrix.com
www.radiometrix.com

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The Intrastat commodity code for all our modules is: 8542 6000

R&TTE Directive

After 7 April 2001 the manufacturer can only place finished product on the market under the provisions of the R&TTE Directive. Equipment within the scope of the R&TTE Directive may demonstrate compliance to the essential requirements specified in Article 3 of the Directive, as appropriate to the particular equipment.
Further details are available on The Office of Communications (Ofcom) web site:
http://www.ofcom.org.uk/

Information Requests
Ofcom
Riverside House
2a Southwark Bridge Road
London SE1 9HA
Tel: +44 (0)300 123 3333 or 020 7981 3040
Fax: +44 (0)20 7981 3333
information.requests@ofcom.org.uk

European Communications Office (ECO)
Peblingehus
Nansensgade 19
DK 1366 Copenhagen
Tel. +45 33896300
Fax +45 33896330
ero@ero.dk
www.ero.dk